Amendments to the Specification

Please add the following replacement paragraphs for paragraphs [0001], [0002], [0030], [0031], and [0033]:

[0001] This application is further related to co-pending U.S. patent application 10/623,397, Attorney Docket No. ONS00501, entitled "VERTICAL COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTOR STRUCTURE", by Peyman Hadizad, assigned to the same assignee, Semiconductor Components Industries, LLC, filed concurrently herewith, and which is incorporated by reference for all purposes.

[0002] This application is related to co-pending U.S. patent application 10/623,390, Attorney Docket No. ONS00502, entitled "DC/DC CONVERTER WITH DEPLETION MODE COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTOR SWITCHING DEVICE", by Peyman Hadizad, assigned to the same assignee, Semiconductor Components Industries, LLC, filed concurrently herewith, and which is incorporated by reference for all purposes.

[0019] Next, a masking, passivation, or dielectric layer 23 is formed or deposited on body of semiconductor material 13. Layer [[13]] 23 provides a means for defining regions for subsequent processing. Preferably, layer 23 comprises a silicon nitride film deposited using plasma-enhanced chemical vapor deposition (PECVD). A thickness on the order of about 0.05 microns to about 0.3 microns is suitable. Layer 23 is then patterned using conventional photolithography and reactive ion etch (RIE) techniques to provide a plurality of openings 24. Preferably, a patterned resist layer (not shown) is left on layer 23 until after a dopant incorporation step, which is described next.

[0022] First trench or groove 36 is then formed in body of semiconductor material 13 through opening 31 and extending from upper surface 19. Trench 36 preferably is formed using reactive ion etching (RIE) or damage free electron cyclotron resonance (ECR) etching, which provides clean and substantially straight sidewall features. A chlorine-based etch chemistry is preferred. Preferably, first trench 36 is between a pair of source regions 26 ~~ach~~ as shown.

[0026] FIG. 5 is an enlarged cross-sectional view of structure 11 after a doped gate region or gate region 59 is formed along at least a portion of sidewalls 53 and bottom surface 54. In the preferred embodiment described herein, gate region 59 comprises a p type dopant, and is formed using ion implantation techniques. Preferably, a dopant species such as beryllium or carbon is used to achieve a p-region depth of about 0.25 microns to about 1.5 microns. To form gate region 59 on sidewalls 53, structure 11 or the implant beam is angled at ~~approximately~~ up to approximately 45 degrees during implantation. Preferably, gate region 59 extends up or covers substantially all of sidewalls 53.

[0035] FIG. 11 shows a cross-sectional view of structure 11 near a final stage of fabrication. A first contact or metal layer 84 is deposited over upper surface 19, and then patterned using conventional techniques. By way of example, first contact layer 84 comprises NiGeAu, NiGeW or other suitable metal to form source contacts. Next, a second contact or metal layer 86 is deposited or plated over first contact layer 84 to provide, among other things, improved contact resistance. Second metal layer 86 comprises nickel or gold, and is deposited using, for example, electroplating or electroless plating techniques.